

taxial layer forming trench **157** formed using the second preliminary trench **155** to be positioned close to the channel region.

Referring to FIG. **11**, the SiGe epitaxial layer **170** is formed in the epitaxial layer forming trench **157**. An epitaxial process for forming the SiGe epitaxial layer **170** may be performed at a temperature in a range of approximately 500 to approximately 900 degrees Centigrade at 1 to 500 Torr, which may be appropriately adjusted within the scope of the invention. In addition,  $\text{SiH}_4$ ,  $\text{SiH}_2\text{Cl}_2$ ,  $\text{SiHCl}_3$ ,  $\text{SiCl}_4$ ,  $\text{SiH}_x\text{Cl}_y$  ( $x+y=4$ ),  $\text{Si}(\text{OC}_4\text{H}_9)_4$ ,  $\text{Si}(\text{OCH}_3)_4$ , or  $\text{Si}(\text{OC}_2\text{H}_5)_4$  may be used as a silicon source gas, and  $\text{GeH}_4$ ,  $\text{GeCl}_4$ , or  $\text{GeH}_x\text{Cl}_y$  ( $x+y=4$ ) may be used as a Ge source gas, but not limited thereto. The SiGe epitaxial layer **170** may be formed by in situ doping of impurity ions.

A top surface of the SiGe epitaxial layer **170** may be formed as high as the top surface of the substrate **100**. Alternatively, as shown in FIG. **12**, the top surface of the SiGe epitaxial layer **171** may be formed to be higher than the top surface of the substrate **100**.

A method of fabricating a semiconductor device according to another embodiment of the present invention will now be described with reference to FIGS. **13** to **15**. FIGS. **13** to **15** are cross-sectional views sequentially illustrating intermediate stages in a method of fabricating a semiconductor device according to another embodiment of the present invention.

Referring to FIG. **13**, the method of fabricating a semiconductor device according to the illustrated embodiment of the present invention is different from the method according to the previous embodiment in that a dummy gate pattern **210**, a dummy gate electrode **220**, and a dummy gate sacrificial layer **230** are used.

Specifically, the dummy gate insulating layer **210**, the dummy gate electrode **220**, and the dummy gate capping layer **230** are formed on the substrate **100**. The dummy gate insulating layer **210** may be formed of a silicon oxide layer. The dummy gate electrode **220** may be made of poly-Si, and the dummy gate capping layer **230** may be made of SiN, or SiON. The reason of using the dummy gate electrode **220** is because processing temperatures of subsequent processes, for example, processes of forming the lightly/heavily doped impurity regions **102** and **103**, are higher than a melting point of a metallic material used for a gate electrode (**320** of FIG. **15**).

Next, the epitaxial layer forming trench **157** is completed by the fabricating method shown in FIGS. **2** to **11**, and the SiGe epitaxial layer **170** is formed in the epitaxial layer forming trench **157**. Subsequently, an interlayer dielectric layer **180** filling the dummy gate pattern **210**, the dummy gate electrode **220**, the dummy gate capping layer **230**, and the spacer **140** can be formed on the substrate **100**, and the interlayer dielectric layer **180** is planarized until a top surface of the dummy gate capping layer **230** is exposed.

Referring to FIG. **14**, the dummy gate insulating layer **210**, the dummy gate electrode **220**, and the dummy gate capping layer **230** are selectively removed to form the gate forming trench **250**. Alternatively, the dummy gate insulating layer **210** may not be removed. The dummy gate insulating layer **210**, the dummy gate electrode **220**, and the dummy gate capping layer **230** may be removed by reactive ion etching.

Referring to FIG. **15**, a gate insulating layer **310**, a gate electrode **320**, and a gate capping layer **330** are formed in the gate forming trench **250**. The gate insulating layer **310** may be made of a high-k material such as  $\text{HfO}_2$ ,  $\text{ZrO}_2$ ,  $\text{Al}_2\text{O}_3$ ,  $\text{Ta}_2\text{O}_5$ , hafnium silicate, zirconium silicate, or a combination thereof. The gate electrode **320** may be made of a metal such as Al, W,

Ta, TaN, TaSiN, TiN, Mo, Ru, Ni, or NiSi. The gate capping layer **130** may be made of SiN, or SiON.

While the present invention has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the spirit and scope of the present invention as defined by the following claims. It is therefore desired that the present embodiments be considered in all respects as illustrative and not restrictive, reference being made to the appended claims rather than the foregoing description to indicate the scope of the invention.

What is claimed is:

1. A method of fabricating a semiconductor device comprising:

forming a gate electrode on a substrate;  
forming a spacer on sidewalls of the gate electrode;  
etching a predetermined portion of the substrate exposed by the spacer and the gate electrode to form a first preliminary trench;  
forming a sacrificial layer on a bottom surface of the first preliminary trench that exposes a sidewall of the first preliminary trench;  
laterally etching the sidewall of the first preliminary trench to form a second preliminary trench;  
removing the sacrificial layer;  
etching the second preliminary trench to form a trench; and  
forming a SiGe epitaxial layer in the trench, wherein the trench has a hexagonal profile;  
wherein etching the second preliminary trench is performed by crystallographic anisotropic etching based on wet etching;  
wherein KOH, NaOH,  $\text{NH}_4\text{OH}$ , or tetramethyl ammonium hydroxide (TMAH) is used as an etching solution in the crystallographic anisotropic etching based on wet etching;  
wherein laterally etching the sidewall of the first preliminary trench comprises laterally etching the sidewall of the first preliminary trench exposes a predetermined portion of a bottom surface of the spacer beneath the substrate; and  
wherein a location on a sidewall of the second preliminary trench defining a maximum width thereof is closer to a top surface of the substrate than a location on the sidewall of the first preliminary trench defining a maximum width thereof.

2. The method of claim 1, wherein the sidewall of the second preliminary trench is closer to a channel region beneath the gate electrode than the sidewall of the first preliminary trench.

3. The method of claim 1, wherein the sacrificial layer comprises a high-density plasma (HDP) oxide layer.

4. The method of claim 3, wherein removing the sacrificial layer comprises sequentially cleaning using  $\text{O}_3\text{HF}$  and plasma native oxide cleaning (PNC) or pre native oxide cleaning.

5. The method of claim 1, wherein a distance from the top surface of the substrate to a tip of a sidewall of the trench is 7 nm or less.

6. The method of claim 5, wherein the tip is aligned with a sidewall of the gate electrode.

7. The method of claim 1, wherein etching the predetermined portion of the substrate comprises etching the predetermined portion of the substrate using an etch back process.

8. The method of claim 1, further comprising:  
forming a lightly doped impurity region by implanting low concentration impurity ions into the substrate using the